Digital Resolver

TYPICAL APPLICATIONS

Wherever precise position data is required for computer input

- Position and velocity sensing
- Brushless DC servo commutation
- Robotics and factory automation
- CNC machine tools
- Material handling
- Medical devices

FEATURES

- Size 11 heavy-duty brushless resolver
- Totally digital input / output
- Absolute position data output
- 12-bit resolution standard
- Maximum system error of ±15 arc minutes
- Incremental encoder with A Quad B and North Marker outputs
- 1024 line incremental resolution standard
- High readout rate
- Mechanical modifications to order

Model DRBB-11-AA-01AA
DC Input / Digital Output

Brushless resolver with built-in electronics that functions as an absolute encoder - DC in / digital out

Moog Components Group's size 11 digital resolver is a compact, low-cost angular position transducer with DC input and digital output. No external circuitry is required – simply energize with ±5 VDC and obtain 12-bit serial data for direct computer interface, or the A Quad B and North Marker outputs of an incremental encoder.

Brushless resolvers are superior to encoders in terms of ruggedness, size, accuracy and resolution. Resolvers perform efficiently under temperature extremes, humidity, shock and vibration.

Model DRBB-11-AA-01AA requires two power supplies and two inputs and provides four outputs, all of which are TTL compatible. RS-422 differential line drivers / receivers and operation from a single 5 volt supply are available options.

SPECIFICATIONS

Dynamic Performance

Rotational speed: 375 rps max. (Intermittent Duty)

Settling Time: 7 ms (1° step) 20 ms (179° step)

Life: 16,000 hours at 80 rps

Mechanical Characteristics

Termination: 12 inch min. #28 AWG (7 / 36) type ET leads in accordance with MIL-W-16878 / 6–BCB. Lead and connector variations available.

Shaft End Play: .0015 max. spring loaded toward front end

Shaft Radial Play: .0005 max. when measured next to bearin with an 8 oz reversing gage load

Input Current: 35 mA

Operating Temperature: -40°C to +85°C

Weight: 142 grams (typ)

Inputs / Outputs And Lead Wire Color Code

	Lead Wire Color	Part Number Base DRBB	DRBD	DRBE	DRBG
Inputs	RED	+5 VDC	+5 VDC	+5 VDC	+5 VDC
	YEL	–5 VDC	–5 VDC	—	—
	BLK	GND	GND	GND	GND
	GRN	$\overline{CS}$	—	—	$\overline{CS}$
	BLU	SCLK	—	—	SCLK
	GRN / RED	—	$\overline{CS}$	$\overline{CS}$	—
	GRN / YEL	—	$\overline{CS}$ comp	$\overline{CS}$ comp	—
	BLU / RED	—	SCLK	SCLK	—
	BLU / YEL	—	SCLK comp	SCLK comp	—
Outputs	RED / WHT	DATA	—	—	DATA
	YEL / WHT	A	—	—	A
	BLU / WHT	B	—	—	B
	BLK / WHT	NM	—	—	NM
	WHT / RED	—	DATA	DATA	—
	WHT / YEL	—	DATA comp	DATA comp	—
	BRN / RED	—	A	A	—
	BRN / YEL	—	A comp	A comp	—
	GRY / RED	—	B	B	—
	GRY / YEL	—	B comp	B comp	—
	VIO / RED	—	NM	NM	—
	VIO / YEL	—	NM comp	NM comp	—
Optional	RED / GRN	VEL	—	—	VEL
	BLK / GRN	DIR	—	—	DIR
	YEL / GRN	NMC	—	—	NMC
	BLU / GRN	CLKOUT	—	—	CLKOUT
	VIO / WHT	NMC	—	—	NMC

Digital Resolver Base Part Number	RS-422 Differential Digital I / O	Single +5 Volt Supply
DRBB-11-AA-01AA	No	No
DRBD-11-AA-01AA	Yes	No
DRBE-11-AA-01AA	Yes	Yes
DRBG-11-AA-01AA	No	Yes

Input / Output Descriptions

Inputs

Voltages: +5 VDC, –5 VDC, Ground

△ $\overline{CS}$: Chip Select. Active LO. Logic transition enables data output.

△ SCLK: Serial interface clock. Data is clocked out on "first" negative edge of SCLK, after a LO transition on $\overline{CS}$. Twelve pulses to clock data out.

Outputs

Standard

Absolute Position

▲△ DATA: Serial Interface Data

(DRBB & DRBG versions) High impedance with $\overline{CS}$=HI

(DRBD & DRBE versions) Data output undefined with $\overline{CS}$=HI

Enabled by $\overline{CS}$=0

Resolution: 12 bits

Max. read rate: 144 K readings / second with 2 MHz serial clock

Logic I / O: Standard TTL or RS-422

Accuracy: 15' max. (resolver plus converter)

Incremental Encoder (1024-line)

▲△ A: Encoder A Output

▲△ B: Encoder B Output

A leads B for increasing angular rotation

Symmetry: 180° ±15°

Quadrature: 90° ±11°

Edge separation: ž550ns at max. > scanning frequency (384 KHz)

▲△ NM: Encoder North Marker emulation output. Pulse triggered as code passes through zero. 90° pulse width (180° and 360° using NMC)

Optional

VEL: Indicates angular velocity of input signals (150 rps / VDC)

Load drive capability: ±250 µA at V_{out} = ±2.5 VDC

NMC: North Marker width Controller (90°, 180°, or 360°)

▲ CLKOUT: Internal VCO clock output; indicates angular velocity of input signals (4 KHz / rps)

▲ DIR: Indicates direction of rotation of input

LOGIC HI = Increasing angular rotation = CW shaft rotation

LOGIC LO = Decreasing angular rotation = CCW shaft rotation

(DRBB & DRBG versions)

▲ NOTE: OUTPUT LOAD CAPABILITY:

Output high voltage: 4 VDC at 1_{OH} = 1 mA

Output low voltage: 1 VDC at 1_{OL} = 1 mA

(DRBD & DRBE versions)

△ NOTE: Digital inputs and outputs meet the requirements of EIA standard RS-422. Signal and Signal compliment are utilized for all digital signals.

TIMING CHARACTERISTICS

Absolute Position Output

Serial Interface

Absolute angular position is represented by serial binary data and is extracted via a three wire interface: DATA, $\overline{CS}$ and SCLK. The DATA output is held in a high impedance state when $\overline{CS}$ is HI.

Upon the application of a LOGIC LO to the $\overline{CS}$ pin. The DATA output is enabled and the current angular information is transferred from the counters to the serial interface. Data is retrieved by appling an external clock to the SCLK pin. The maximum data rate of the SCLK is 2 MHz. To ensure secure data retrieval it is important to note that SCLK should not be applied until a minimum period of 600 ns after the application of a LOGIC LO to $\overline{CS}$.

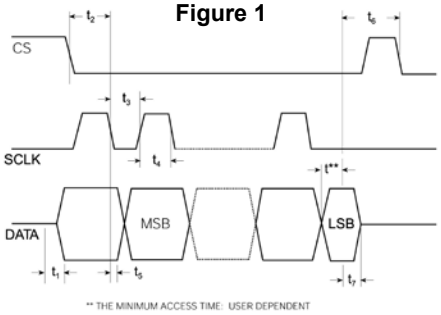
Data is then clocked out, MSB first. On successive negative edges of the SCLK: 12 clock edges are required to extract the full 12 bits of data. Subsequent negtive edges greater than the defined resolution of the converter will clock zeros from the data output if $\overline{CS}$ remains in a low state.

If a resolution of less than 12 bits is required, the data access can be terminated by releasing $\overline{CS}$ after the required number of bits have been read.

$\overline{CS}$ can be released a minimum of 100ns after the last negative edge. If the user is reading data continuously, $\overline{CS}$ can be reapplied a minimum of 250ns after it is released (see Figure 1).

The maximum read time is given by: (12-bits read @ 2 MHz) MAX RD TIME = [600 + (12 x 500) + 250 +100] = 6.95 µs

Figure 1



Parameter	Units	Test Conditions / Notes
t_1	150 ns Max.	$\overline{CS}$ to DATA enable
t_2	600 ns Min.	$\overline{CS}$ to ist SCLK negative edge
t_3	250 ns Min.	SCLK low pulse
t_4	250 ns Min.	SCLK high pulse
t_5	100 ns Max.	SCLK negative edge to DATA valid
t_6	250 ns Min.	$\overline{CS}$ high pulse width
t_7	150 ns Max.	$\overline{CS}$ high to DATA high Z (BUS Relinquish)

SCLK can only be applyed after t_2 has elapsed.

NOTES:
1. Timing data are not 100% production tested. Sample tested at +25°C only to ensure conformance to data sheet limits. Logic output timing tests carried out using 10pF, 100ka load.
2. Capacitance of DATA pin in high impedance state = 15 pF.

Incremental Encoder Output

The Incremental encoder emulation outputs A, B and NM are free running and are always valid.

The digital resolver emulates a 1024-line encoder. Relating this to converter resolution means one revolution produces 1024, A, B Pulses. A leads B for increasing angular rotation. The addition of the DIR output negates the need for external A and B direction decode logic. DIR is HI for increasing angular rotation (CW shaft rotation).

The North Marker Pulse is generated as the absolute angular position passes through zero. The digital rsolver supports the three industry standard widths controlled using the NMC pin. Figure 2 details the relationship between A, B and NM. The width of NM is defined relative to the A cycle.

Unlike the incremental encoders, the digital resolver output is not subject to error specifications such as cycle error, eccentricity, pulse and state width errors, count density and pulse error.

The maximum speed rating, N, of an encoder is calculated from its maximum switching frequency, F_{MAX}, and its PPR (Pulse Per Revolution).

$$n = \frac{60 \times F_{MAX}}{PPR}$$

The digital resolver A, B pulses are initiated from CLKOUT which has a maximum frequency of 1.536 MHz. The equivalent encoder switching frequency is:

1/4 x 1.536 MHz = 384 kHz (4 UPDATES = 1 PULSE)

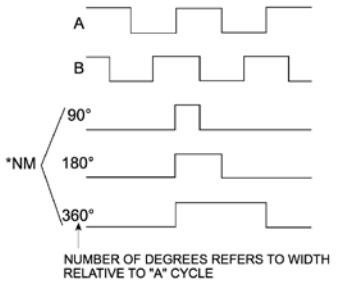
At 12 bits the PPR = 1024. Therefore the maximum speed, N, of the digital resolver is:

$$n = \frac{60 \times 384000}{1024} = 22500 \text{ rpm}$$

This compares favorably with encoder specifications where F_{MAX} is specified from 20 kHz (photo diodes) to 125 kHz (laser based) depending on the light system used. A 1024 line laser-based encoder will have a maximum speed of 7300 rpm.

The inclusion of A, B outputs allows the digital resolver solution to replace optical encoders directly without the need to change or upgrade existing application software.

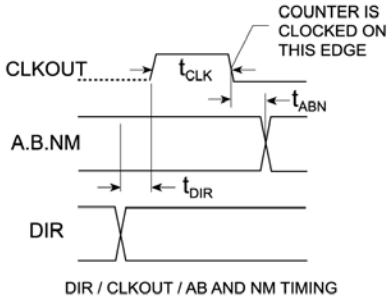
Figure 2



Level	Width
+5 VDC	90°
0	180°
-5 VDC	360°

*Selectable with three - level control pin “marker” default to 90° using internal pull-up.

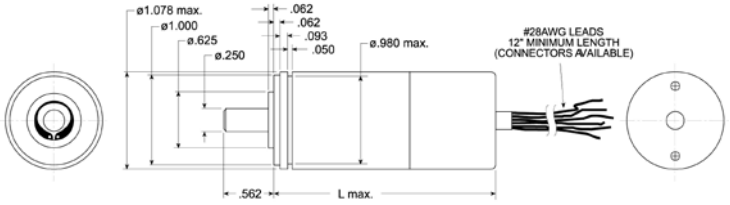
DIMENSIONS



DIR / CLKOUT / AB AND NM TIMING

Parameter	Min.	Max.	Units	Test Conditions / Notes
t_{DIR}		200	ns	DIR to CLKOUT positive edge
t_{CLK}	250	400	ns	CLKOUT Pulse width
t_{ABN}		250	ns	CLKOUT negative edge to A, B and NM transition

Digital Resolver Dimensions



Dimensions are in inches

	DRBB	DRBD	DRBE	DRBG
L_{MAX}	2.443	2.827	2.943	2.827